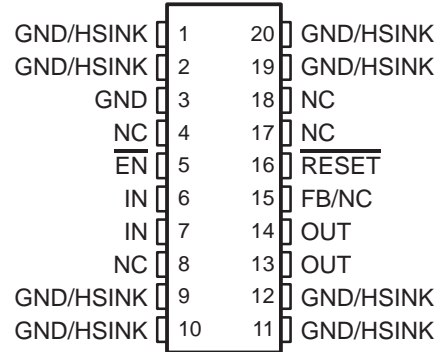


- 1 A Low-Dropout Voltage Regulator
- Available in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V, 5.0-V Fixed Output and Adjustable Versions
- Dropout Voltage Down to 230 mV at 1 A (TPS76750)
- Ultralow 85 μ A Typical Quiescent Current
- Fast Transient Response
- 2% Tolerance Over Specified Conditions for Fixed-Output Versions
- Open Drain Power-On Reset With 200-ms Delay (See TPS768xx for PG Option)
- 8-Pin SOIC and 20-Pin TSSOP PowerPAD™ (PWP) Package
- Thermal Shutdown Protection

description

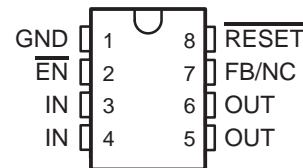
This device is designed to have a fast transient response and be stable with 10 μ F low ESR capacitors. This combination provides high performance at a reasonable cost.

PWP PACKAGE
(TOP VIEW)

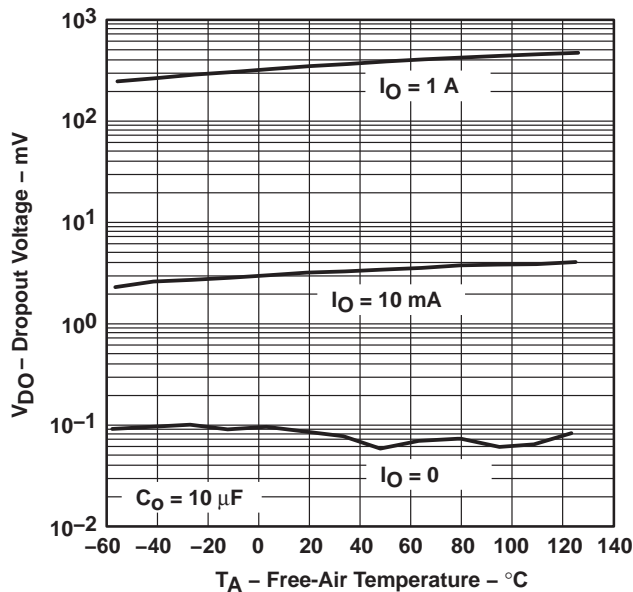


NC – No internal connection

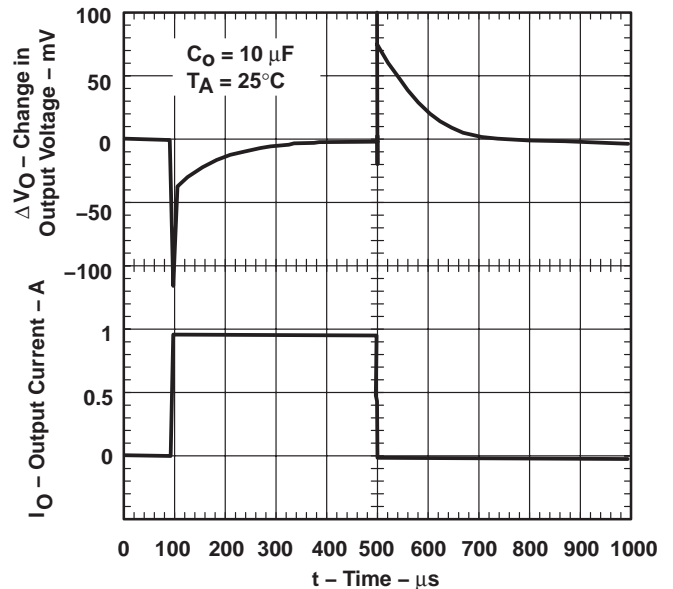
D PACKAGE
(TOP VIEW)



TPS76733
DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE



TPS76733
LOAD TRANSIENT RESPONSE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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**TPS76715Q, TPS76718Q, TPS76725Q, TPS76727Q
 TPS76728Q, TPS76730Q, TPS76733Q, TPS76750Q, TPS76701Q
 FAST-TRANSIENT-RESPONSE 1-A LOW-DROPOUT LINEAR REGULATORS**

SLVS208I – MAY 1999 – REVISED JANUARY 2004

description (continued)

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 230 mV at an output current of 1 A for the TPS76750) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 85 μ A over the full range of output current, 0 mA to 1 A). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a sleep mode; applying a TTL high signal to $\overline{\text{EN}}$ (enable) shuts down the regulator, reducing the quiescent current to 1 μ A at $T_J = 25^\circ\text{C}$.

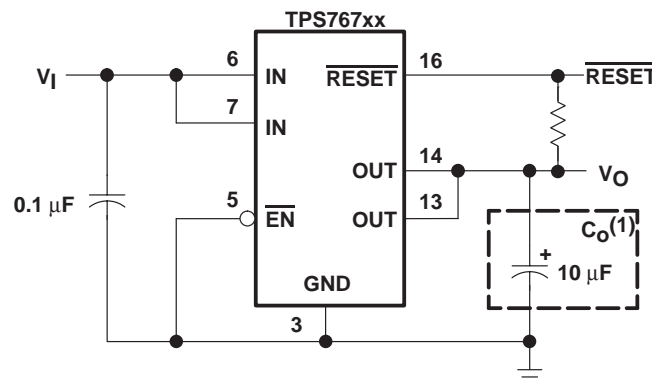
The $\overline{\text{RESET}}$ output of the TPS767xx initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS767xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage.

The TPS767xx is offered in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V, and 5.0-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5 V to 5.5 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS767xx family is available in 8-pin SOIC and 20-pin PWP packages.

AVAILABLE OPTIONS

| T_J | OUTPUT VOLTAGE (V) | PACKAGED DEVICES | |
|----------------|------------------------------|------------------|-----------|
| | TYP | TSSOP (PWP) | SOIC (D) |
| -40°C to 125°C | 5.0 | TPS76750Q | TPS76750Q |
| | 3.3 | TPS76733Q | TPS76733Q |
| | 3.0 | TPS76730Q | TPS76730Q |
| | 2.8 | TPS76728Q | TPS76728Q |
| | 2.7 | TPS76727Q | TPS76727Q |
| | 2.5 | TPS76725Q | TPS76725Q |
| | 1.8 | TPS76718Q | TPS76718Q |
| | 1.5 | TPS76715Q | TPS76715Q |
| | Adjustable 1.5 V to 5.5 V | TPS76701Q | TPS76701Q |

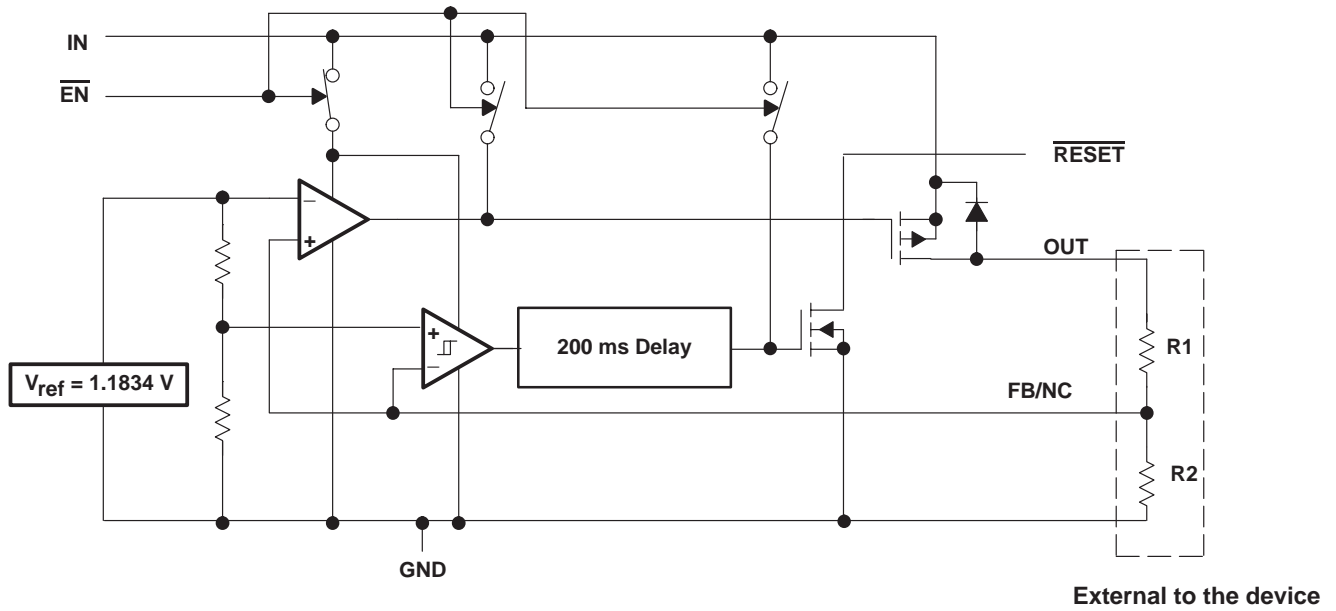
The TPS76701 is programmable using an external resistor divider (see application information). The D and PWP packages are available taped and reeled. Add an R suffix to the device type (e.g., TPS76701QDR).



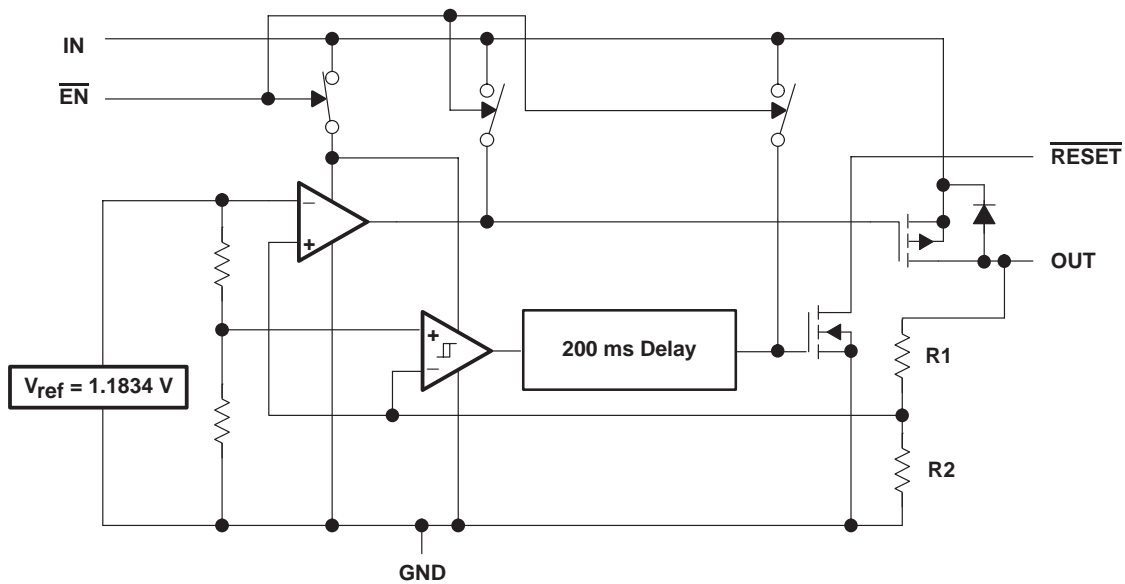
(1) See application information section for capacitor selection details.

Figure 1. Typical Application Configuration (For Fixed Output Options)

functional block diagram—adjustable version



functional block diagram—fixed-voltage version



Terminal Functions

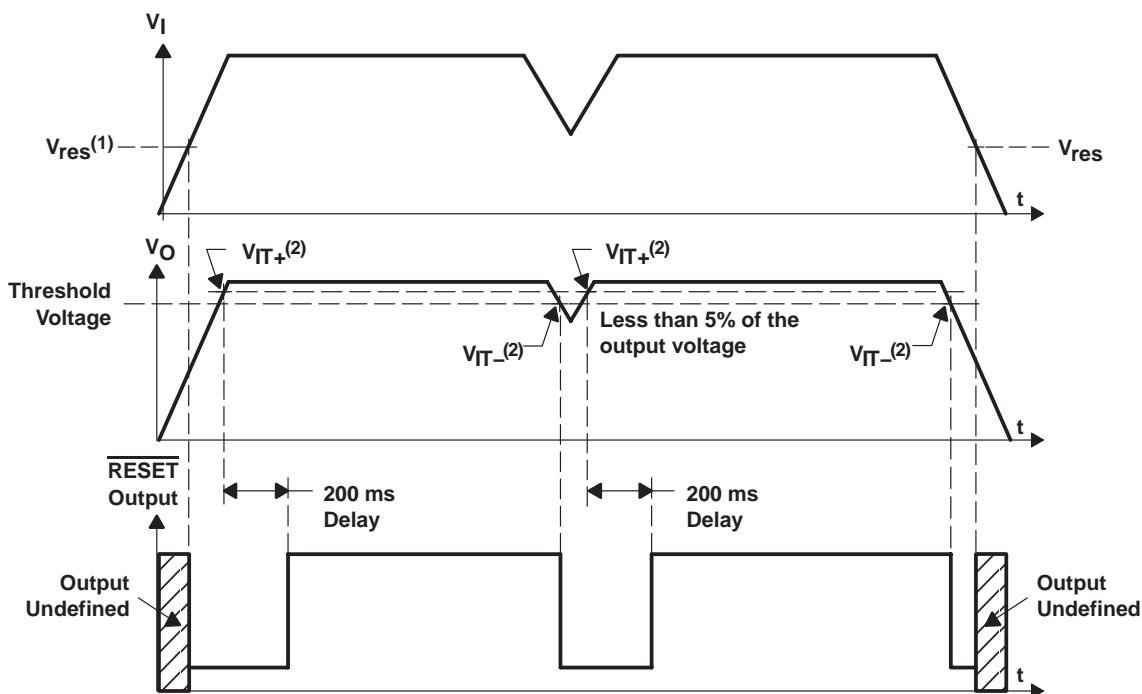
SOIC Package

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|---------------------------|------|-----|-----------------------------------------------------------------------------|
| $\overline{\text{EN}}$ | 2 | I | Enable input |
| FB/NC | 7 | I | Feedback input voltage for adjustable device (no connect for fixed options) |
| GND | 1 | | Regulator ground |
| IN | 3, 4 | I | Input voltage |
| OUT | 5, 6 | O | Regulated output voltage |
| $\overline{\text{RESET}}$ | 8 | O | $\overline{\text{RESET}}$ output |

PWP Package

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|---------------------------|-----------------------------|-----|-----------------------------------------------------------------------------|
| $\overline{\text{EN}}$ | 5 | I | Enable input |
| FB/NC | 15 | I | Feedback input voltage for adjustable device (no connect for fixed options) |
| GND | 3 | | Regulator ground |
| GND/HSINK | 1, 2, 9, 10, 11, 12, 19, 20 | | Ground/heatsink |
| IN | 6, 7 | I | Input voltage |
| NC | 4, 8, 17, 18 | | No connect |
| OUT | 13, 14 | O | Regulated output voltage |
| $\overline{\text{RESET}}$ | 16 | O | $\overline{\text{RESET}}$ output |

timing diagram



(1) V_{res} is the minimum input voltage for a valid $\overline{\text{RESET}}$. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

(2) V_{IT-} - Trip voltage is typically 5% lower than the output voltage ($95\%V_O$) V_{IT-} to V_{IT+} is the hysteresis voltage.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | |
|---------------------------------------------------|-------------------------------|
| Input voltage range ⁽²⁾ , V_I | -0.3 V to 13.5 V |
| Voltage range at \overline{EN} | -0.3 V to $V_I + 0.3$ V |
| Maximum \overline{RESET} voltage | 16.5 V |
| Peak output current | Internally limited |
| Output voltage, V_O (OUT, FB) | 7 V |
| Continuous total power dissipation | See dissipation rating tables |
| Operating junction temperature range, T_J | -40°C to 125°C |
| Storage temperature range, T_{stg} | -65°C to 150°C |
| ESD rating, HBM | 2 kV |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURES

| PACKAGE | AIR FLOW (CFM) | $T_A < 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$ POWER RATING | $T_A = 85^\circ\text{C}$ POWER RATING |
|---------|----------------|------------------------------------------|---------------------------------------------------|------------------------------------------|------------------------------------------|
| D | 0 | 568 mW | 5.68 mW/°C | 312 mW | 227 mW |
| | 250 | 904 mW | 9.04 mW/°C | 497 mW | 361 mW |

DISSIPATION RATING TABLE 2 – FREE-AIR TEMPERATURES

| PACKAGE | AIR FLOW (CFM) | $T_A < 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$ POWER RATING | $T_A = 85^\circ\text{C}$ POWER RATING |
|---------|----------------|------------------------------------------|---------------------------------------------------|------------------------------------------|------------------------------------------|
| PWP§ | 0 | 2.9 W | 23.5 mW/°C | 1.9 W | 1.5 W |
| | 300 | 4.3 W | 34.6 mW/°C | 2.8 W | 2.2 W |
| PWP¶ | 0 | 3 W | 23.8 mW/°C | 1.9 W | 1.5 W |
| | 300 | 7.2 W | 57.9 mW/°C | 4.6 W | 3.8 W |

(1) This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 5 in × 5 in PCB, 1 oz. copper, 2 in × 2 in coverage (4 in²).

(2) This parameter is measured with the recommended copper heat sink pattern on a 8-layer PCB, 1.5 in × 2 in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in²) and layers 3 and 6 at 100% coverage (6 in²). For more information, refer to TI technical brief SLMA002.

recommended operating conditions

| | MIN | MAX | UNIT |
|------------------------------------------------------|-----|-----|------|
| Input voltage, V_I ⁽¹⁾ | 2.7 | 10 | V |
| Output voltage range, V_O | 1.2 | 5.5 | V |
| Output current, I_O ⁽²⁾ | 0 | 1.0 | A |
| Operating junction temperature, T_J ⁽²⁾ | -40 | 125 | °C |

(1) Maximum $V_{IN} = V_{OUT} + V_{DO}$ or 2.7V, whichever is greater.

(2) Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

TPS76715Q, TPS76718Q, TPS76725Q, TPS76727Q
TPS76728Q, TPS76730Q, TPS76733Q, TPS76750Q, TPS76701Q
FAST-TRANSIENT-RESPONSE 1-A LOW-DROPOUT LINEAR REGULATORS



SLVS2081 – MAY 1999 – REVISED JANUARY 2004

**electrical characteristics over recommended operating free-air temperature range,
 $V_I = V_O(\text{typ}) + 1 \text{ V}$, $I_O = 1 \text{ mA}$, $\overline{\text{EN}} = 0 \text{ V}$, $C_O = 10 \mu\text{F}$ (unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------|--------------------------------|-------|-----------|----------------------------|
| Output voltage (10 μA to 1 A load) | TPS76701 | $1.5 \text{ V} \leq V_O \leq 5.5 \text{ V}$, $T_J = 25^\circ\text{C}$ | V_O | | | V |
| | | $1.5 \text{ V} \leq V_O \leq 5.5 \text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C | $0.98V_O$ | | $1.02V_O$ | |
| | TPS76715 | $T_J = 25^\circ\text{C}$, $2.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$ | 1.5 | | | |
| | | $T_J = -40^\circ\text{C}$ to 125°C , $2.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$ | 1.470 | | 1.530 | |
| | TPS76718 | $T_J = 25^\circ\text{C}$, $2.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$ | 1.8 | | | |
| | | $T_J = -40^\circ\text{C}$ to 125°C , $2.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$ | 1.764 | | 1.836 | |
| | TPS76725 | $T_J = 25^\circ\text{C}$, $3.5 \text{ V} < V_{\text{IN}} < 10 \text{ V}$ | 2.5 | | | |
| | | $T_J = -40^\circ\text{C}$ to 125°C , $3.5 \text{ V} < V_{\text{IN}} < 10 \text{ V}$ | 2.450 | | 2.550 | |
| | TPS76727 | $T_J = 25^\circ\text{C}$, $3.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$ | 2.7 | | | |
| | | $T_J = -40^\circ\text{C}$ to 125°C , $3.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$ | 2.646 | | 2.754 | |
| | TPS76728 | $T_J = 25^\circ\text{C}$, $3.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$ | 2.8 | | | |
| | | $T_J = -40^\circ\text{C}$ to 125°C , $3.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$ | 2.744 | | 2.856 | |
| | TPS76730 | $T_J = 25^\circ\text{C}$, $4.0 \text{ V} < V_{\text{IN}} < 10 \text{ V}$ | 3.0 | | | |
| | | $T_J = -40^\circ\text{C}$ to 125°C , $4.0 \text{ V} < V_{\text{IN}} < 10 \text{ V}$ | 2.940 | | 3.060 | |
| | TPS76733 | $T_J = 25^\circ\text{C}$, $4.3 \text{ V} < V_{\text{IN}} < 10 \text{ V}$ | 3.3 | | | |
| | | $T_J = -40^\circ\text{C}$ to 125°C , $4.3 \text{ V} < V_{\text{IN}} < 10 \text{ V}$ | 3.234 | | 3.366 | |
| TPS76750 | $T_J = 25^\circ\text{C}$, $6.0 \text{ V} < V_{\text{IN}} < 10 \text{ V}$ | 5.0 | | | | |
| | $T_J = -40^\circ\text{C}$ to 125°C , $6.0 \text{ V} < V_{\text{IN}} < 10 \text{ V}$ | 4.900 | | 5.100 | | |
| Quiescent current (GND current) $\overline{\text{EN}} = 0 \text{ V}$ | | $10 \mu\text{A} < I_O < 1 \text{ A}$, $T_J = 25^\circ\text{C}$ | 85 | | | μA |
| | | $I_O = 1 \text{ A}$, $T_J = -40^\circ\text{C}$ to 125°C | 125 | | | |
| Output voltage line regulation ($\Delta V_O/V_O$) | | $V_O + 1 \text{ V} < V_I \leq 10 \text{ V}$, $T_J = 25^\circ\text{C}$ | 0.01 | | | %/V |
| Load regulation | | | 3 | | | mV |
| Output noise voltage (TPS76718) | | $\text{BW} = 200 \text{ Hz}$ to 100 kHz , $I_O = 1 \text{ A}$, $C_O = 10 \mu\text{F}$, $T_J = 25^\circ\text{C}$ | 55 | | | μV_{rms} |
| Output current limit | | $V_O = 0 \text{ V}$ | 1.2 | 1.7 | 2 | A |
| Thermal shutdown junction temperature | | | 150 | | | $^\circ\text{C}$ |
| Standby current | | $\overline{\text{EN}} = V_I$, $T_J = 25^\circ\text{C}$, $2.7 \text{ V} < V_I < 10 \text{ V}$ | 1 | | | μA |
| | | $\overline{\text{EN}} = V_I$, $T_J = -40^\circ\text{C}$ to 125°C , $2.7 \text{ V} < V_I < 10 \text{ V}$ | 10 | | | μA |
| FB input current | TPS76701 | $\text{FB} = 1.5 \text{ V}$ | 2 | | | nA |
| High level enable input voltage | | | 1.7 | | | V |
| Low level enable input voltage | | | 0.9 | | | V |
| Power supply ripple rejection | | $f = 1 \text{ KHz}$, $T_J = 25^\circ\text{C}$ | $C_O = 10 \mu\text{F}$, 60 | | | dB |

electrical characteristics over recommended operating free-air temperature range,
 $V_I = V_{O(\text{typ})} + 1 \text{ V}$, $I_O = 1 \text{ mA}$, $\overline{\text{EN}} = 0 \text{ V}$, $C_O = 10 \mu\text{F}$ (unless otherwise noted) (continued)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------------------|-----------------------------------------------------------|------------------------------------------------------------------------|-----|------|-----|---------------|
| Reset | Minimum input voltage for valid $\overline{\text{RESET}}$ | $I_O(\text{RESET}) = 300 \mu\text{A}$ | | 1.1 | | V |
| | Trip threshold voltage | V_O decreasing | 92 | | 98 | % V_O |
| | Hysteresis voltage | Measured at V_O | | 0.5 | | % V_O |
| | Output low voltage | $V_I = 2.7 \text{ V}$, $I_O(\text{RESET}) = 1 \text{ mA}$ | | 0.15 | 0.4 | V |
| | Leakage current | $V(\text{RESET}) = 5 \text{ V}$ | | | 1 | μA |
| | RESET time-out delay | | | 200 | | ms |
| Input current ($\overline{\text{EN}}$) | | $\overline{\text{EN}} = 0 \text{ V}$ | -1 | 0 | 1 | μA |
| | | $\overline{\text{EN}} = V_I$ | -1 | | 1 | |
| Dropout voltage (1) | TPS76728 | $I_O = 1 \text{ A}$, $T_J = 25^\circ\text{C}$ | | 500 | | mV |
| | | $I_O = 1 \text{ A}$, $T_J = -40^\circ\text{C}$ to 125°C | | | 825 | |
| | TPS76730 | $I_O = 1 \text{ A}$, $T_J = 25^\circ\text{C}$ | | 450 | | |
| | | $I_O = 1 \text{ A}$, $T_J = -40^\circ\text{C}$ to 125°C | | | 675 | |
| | TPS76733 | $I_O = 1 \text{ A}$, $T_J = 25^\circ\text{C}$ | | 350 | | |
| | | $I_O = 1 \text{ A}$, $T_J = -40^\circ\text{C}$ to 125°C | | | 575 | |
| | TPS76750 | $I_O = 1 \text{ A}$, $T_J = 25^\circ\text{C}$ | | 230 | | |
| | | $I_O = 1 \text{ A}$, $T_J = -40^\circ\text{C}$ to 125°C | | | 380 | |

(1) V_I voltage equals $V_{O(\text{typ})} - 100 \text{ mV}$; TPS76701 output voltage set to 3.3 V nominal with external resistor divider. TPS76715, TPS76718, TPS76725, and TPS76727 dropout voltage limited by input voltage range limitations (i.e., TPS76730 input voltage needs to drop to 2.9 V for purpose of this test).

TYPICAL CHARACTERISTICS

Table of Graphs

| | | | FIGURE |
|----------|------------------------------------|-------------------------|------------------|
| V_O | Output voltage | vs Output current | 2, 3, 4 |
| | | vs Free-air temperature | 5, 6, 7 |
| | Ground current | vs Free-air temperature | 8, 9 |
| | Power supply ripple rejection | vs Frequency | 10 |
| | Output spectral noise density | vs Frequency | 11 |
| | Input voltage (min) | vs Output voltage | 12 |
| Z_O | Output impedance | vs Frequency | 13 |
| V_{DO} | Dropout voltage | vs Free-air temperature | 14 |
| | Line transient response | | 15, 17 |
| | Load transient response | | 16, 18 |
| V_O | Output voltage | vs Time | 19 |
| | | Dropout voltage | vs Input voltage |
| | Equivalent series resistance (ESR) | vs Output current | 22 – 25 |

TYPICAL CHARACTERISTICS

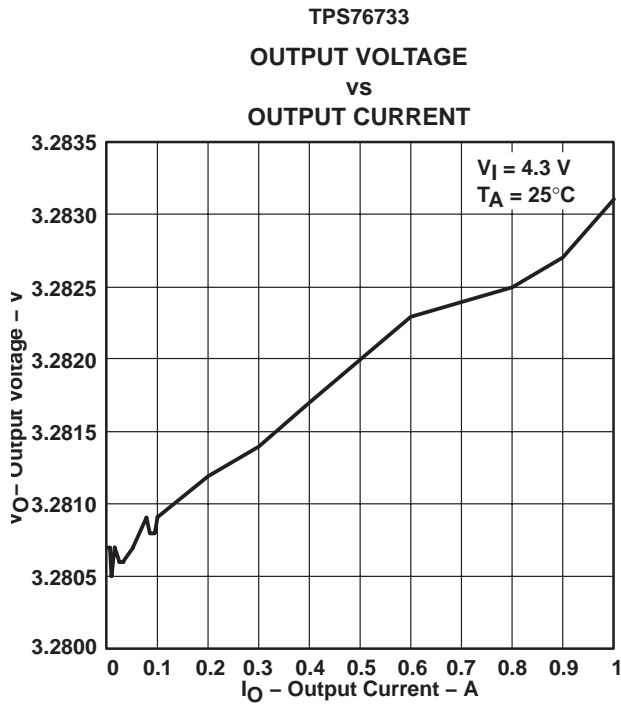


Figure 2

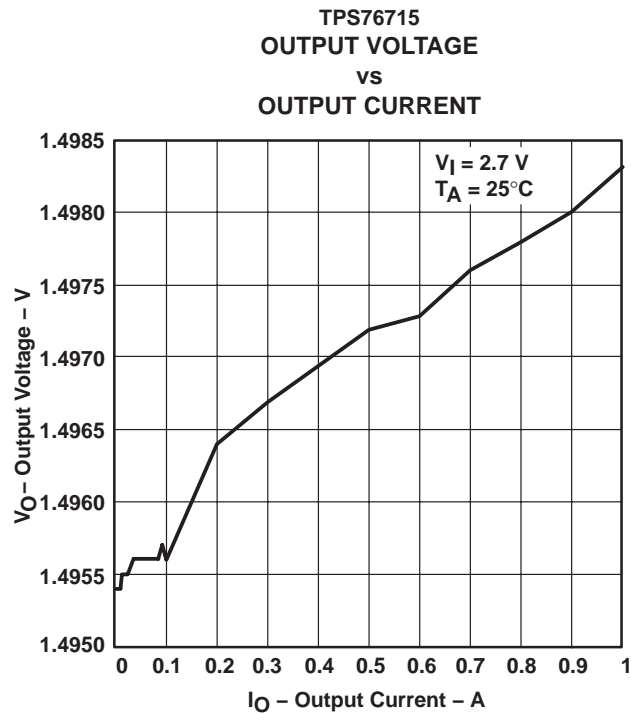


Figure 3

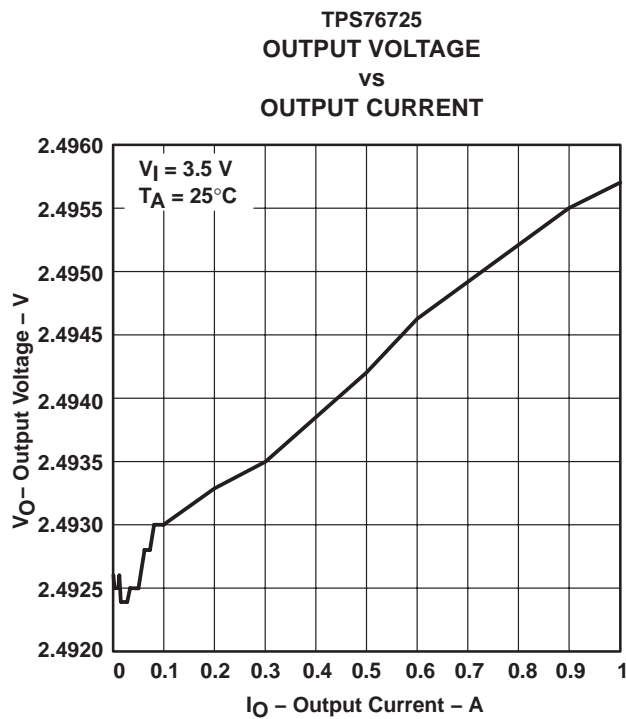


Figure 4

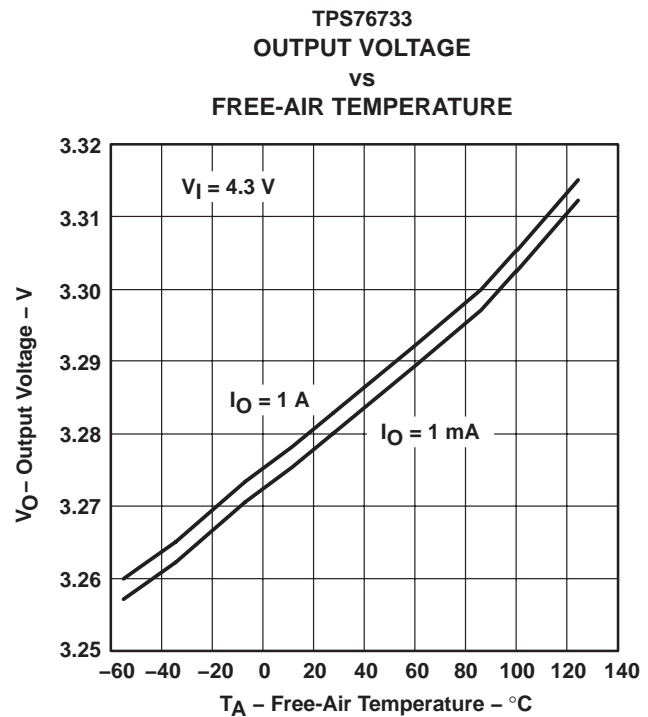


Figure 5

TYPICAL CHARACTERISTICS

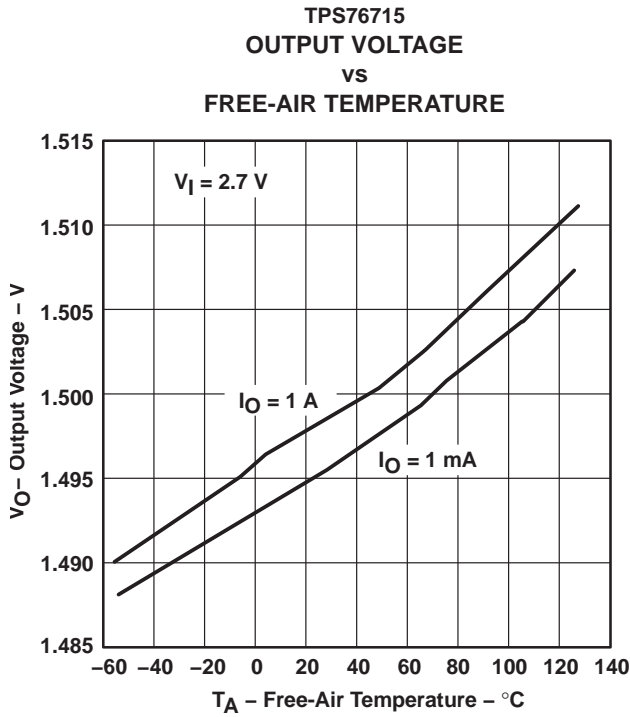


Figure 6

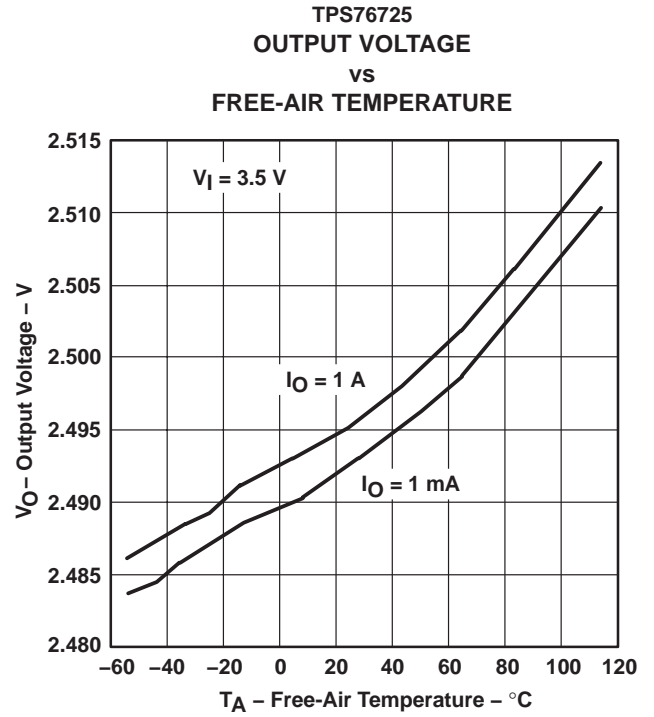


Figure 7

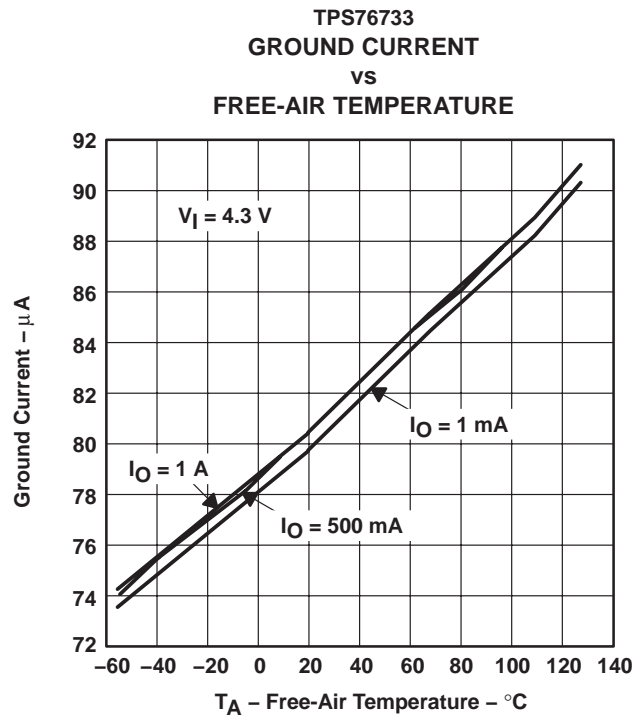


Figure 8

TYPICAL CHARACTERISTICS

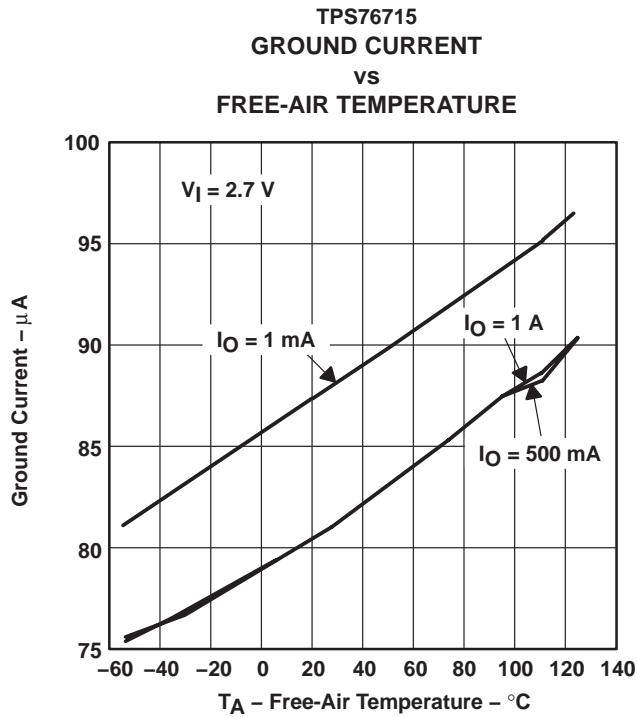


Figure 9

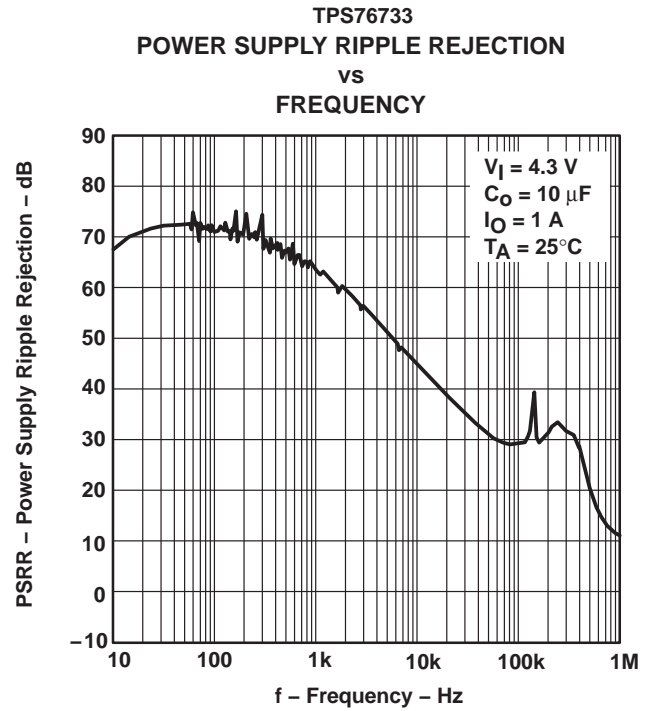


Figure 10

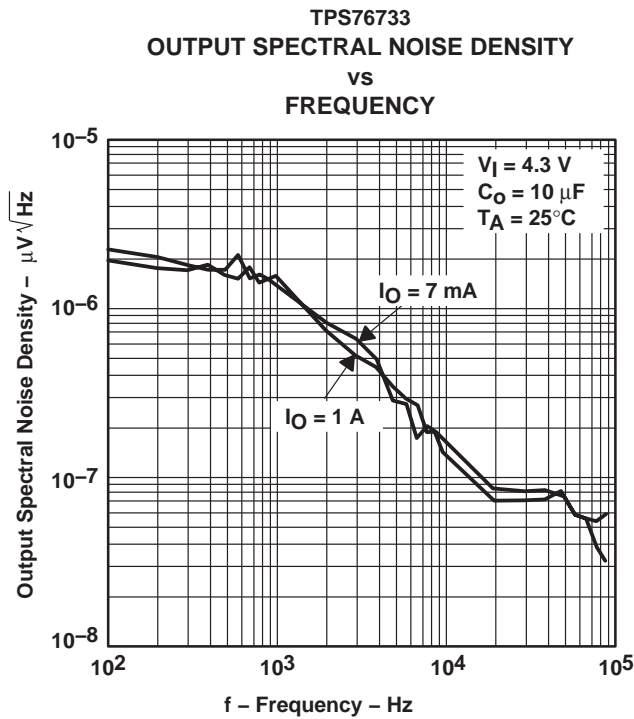


Figure 11

TYPICAL CHARACTERISTICS

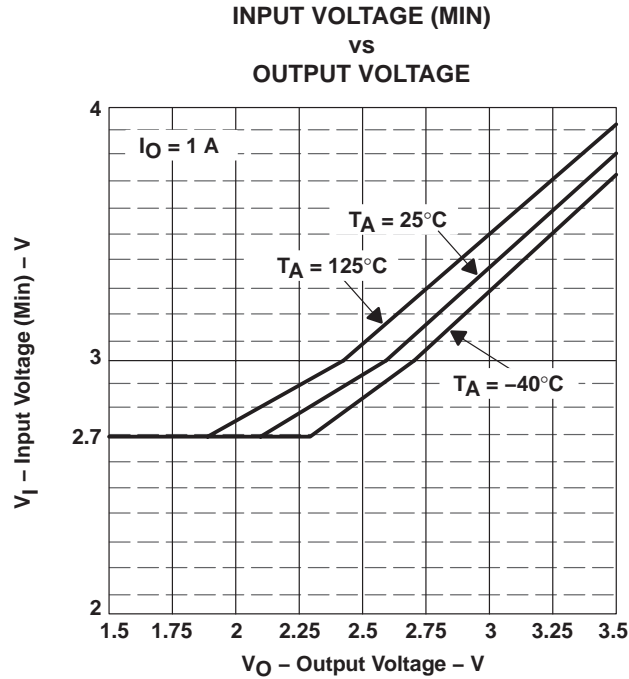


Figure 12

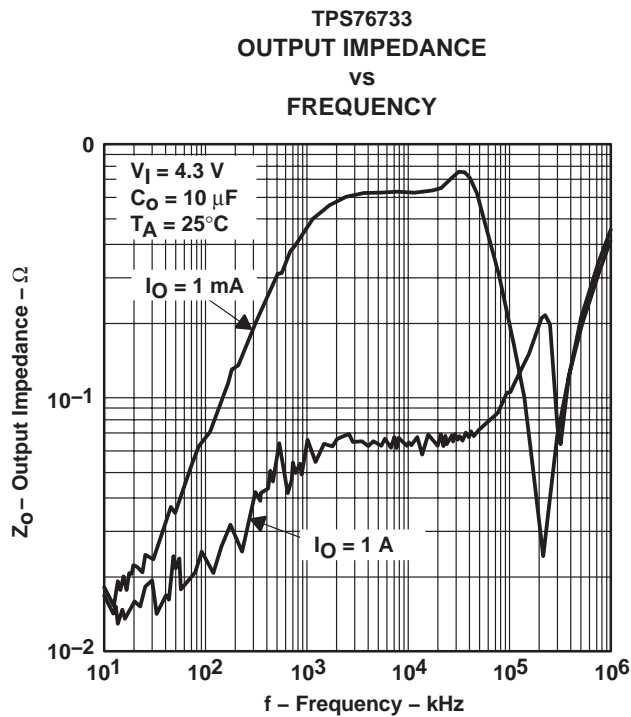


Figure 13

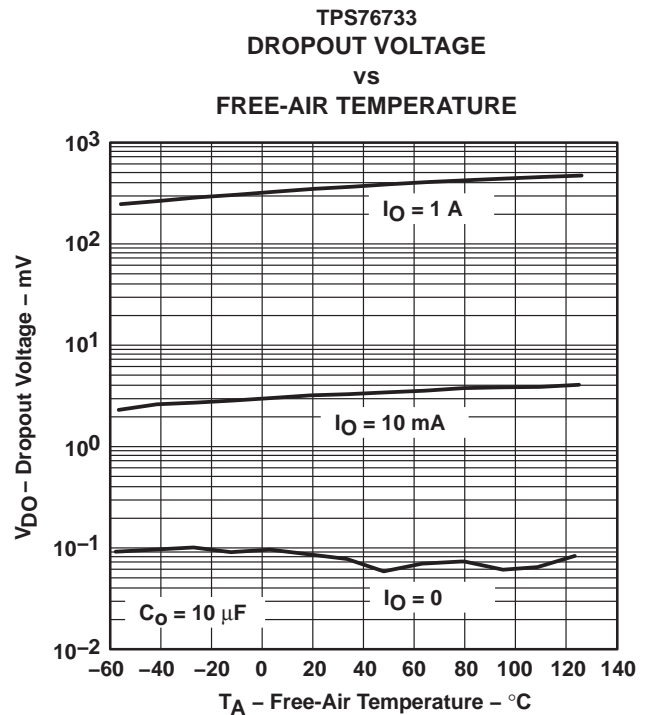


Figure 14

TYPICAL CHARACTERISTICS

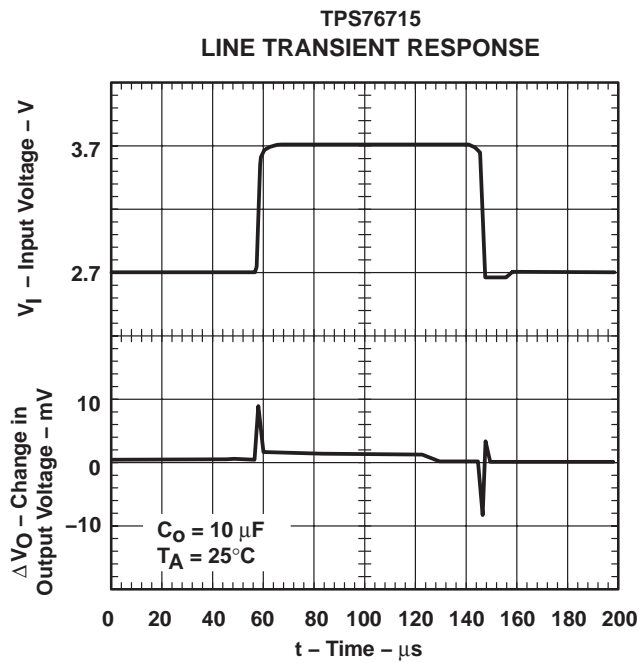


Figure 15

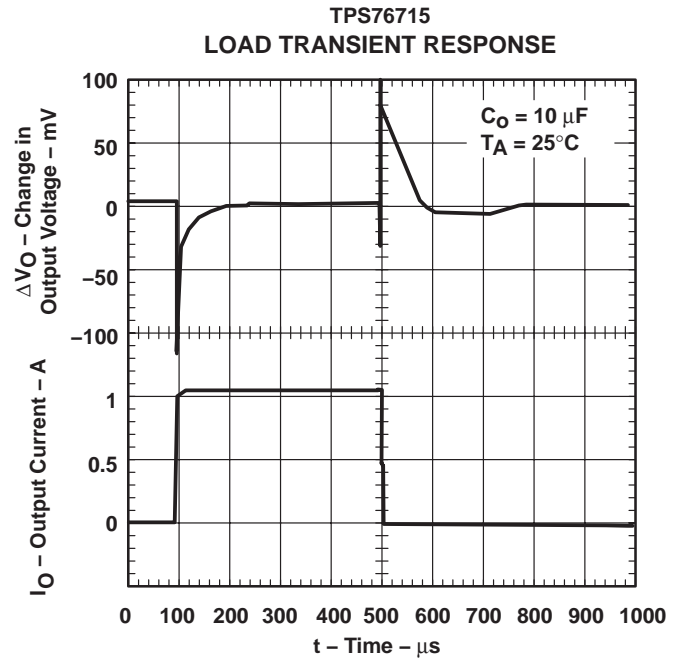


Figure 16

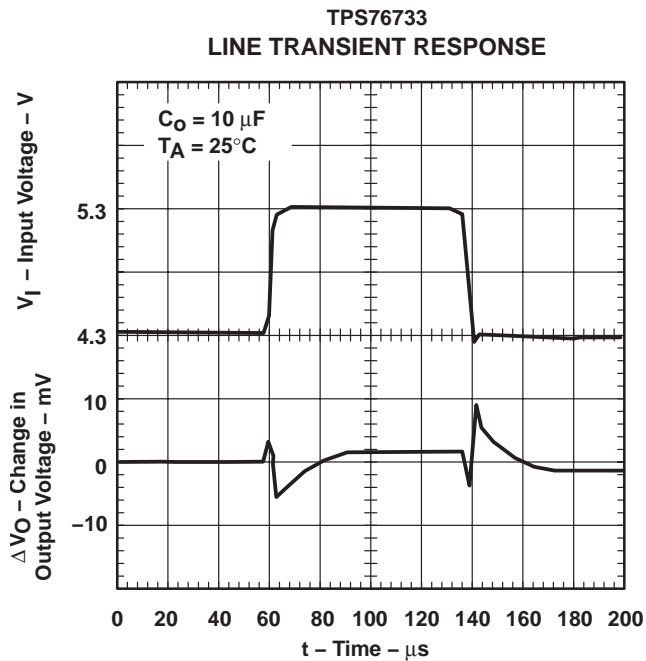


Figure 17

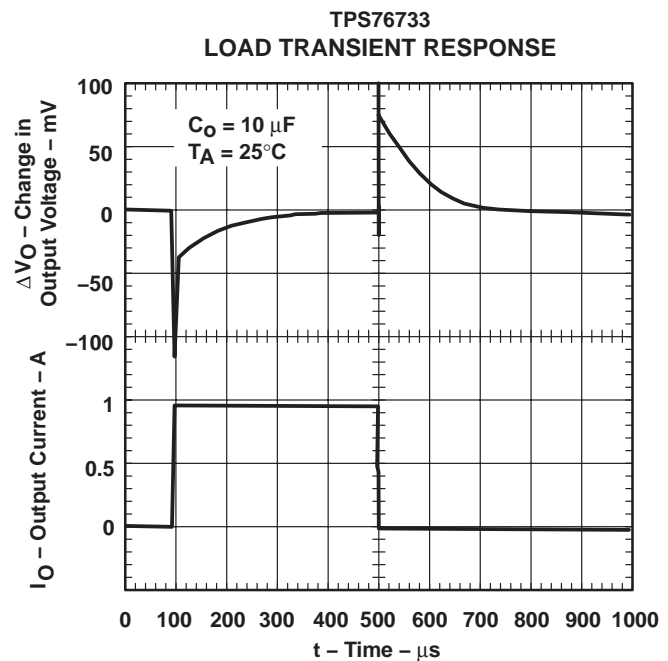


Figure 18

TYPICAL CHARACTERISTICS

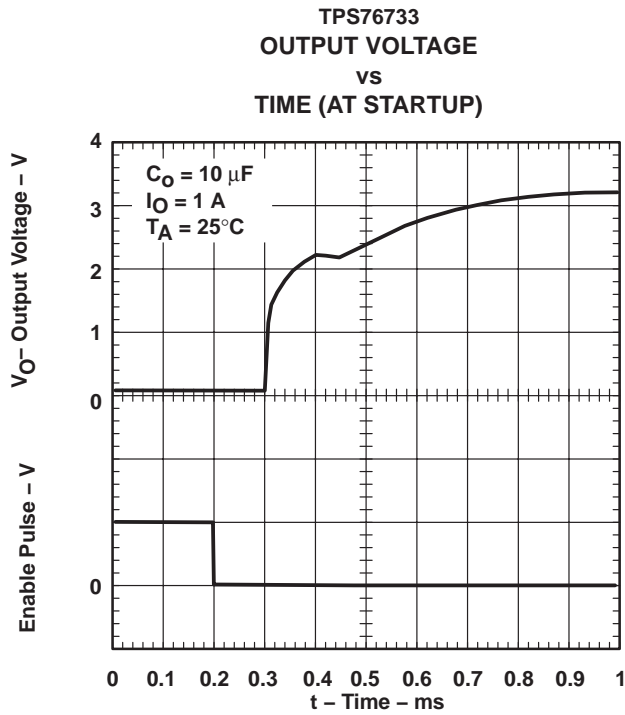


Figure 19

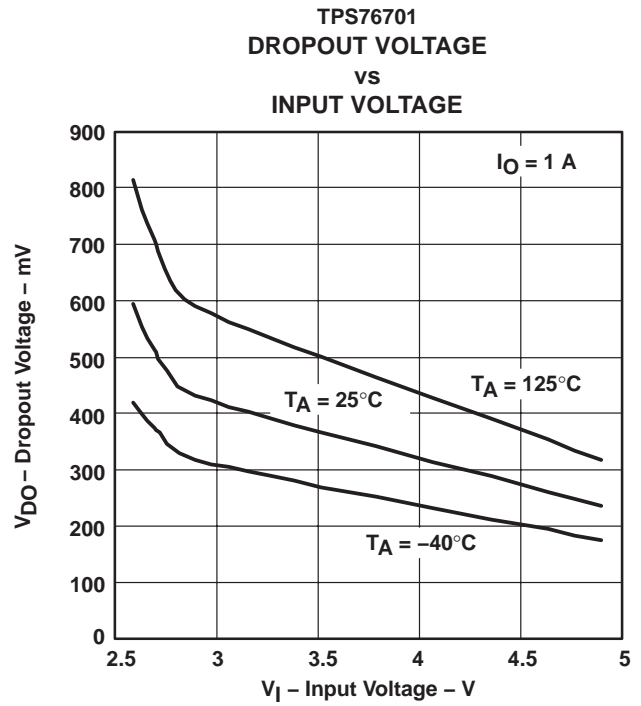


Figure 20

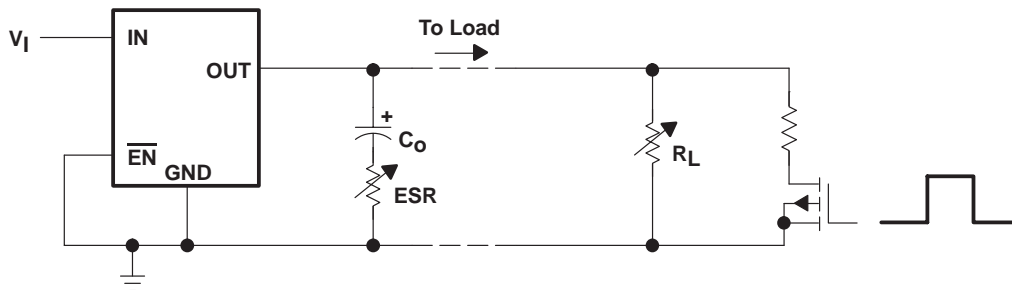


Figure 21. Test Circuit for Typical Regions of Stability (Figures 22 through 25) (Fixed Output Options)

TYPICAL CHARACTERISTICS

TYPICAL REGION OF STABILITY
 EQUIVALENT SERIES RESISTANCE(1)
 vs
 OUTPUT CURRENT

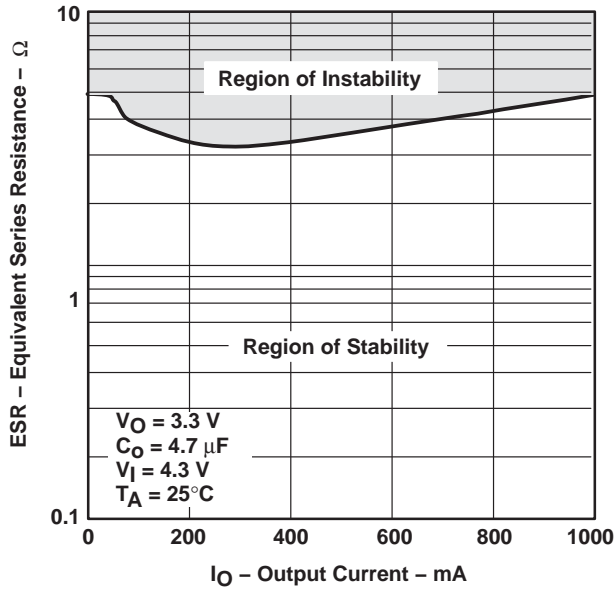


Figure 22

TYPICAL REGION OF STABILITY
 EQUIVALENT SERIES RESISTANCE(1)
 vs
 OUTPUT CURRENT

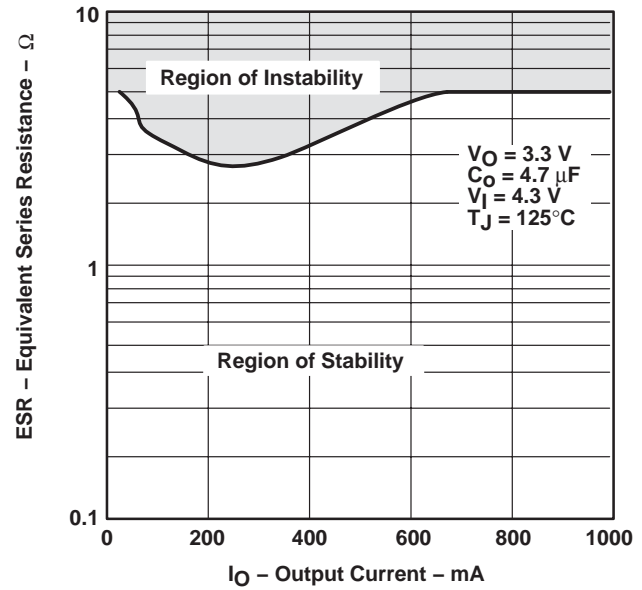


Figure 23

TYPICAL REGION OF STABILITY
 EQUIVALENT SERIES RESISTANCE(1)
 vs
 OUTPUT CURRENT

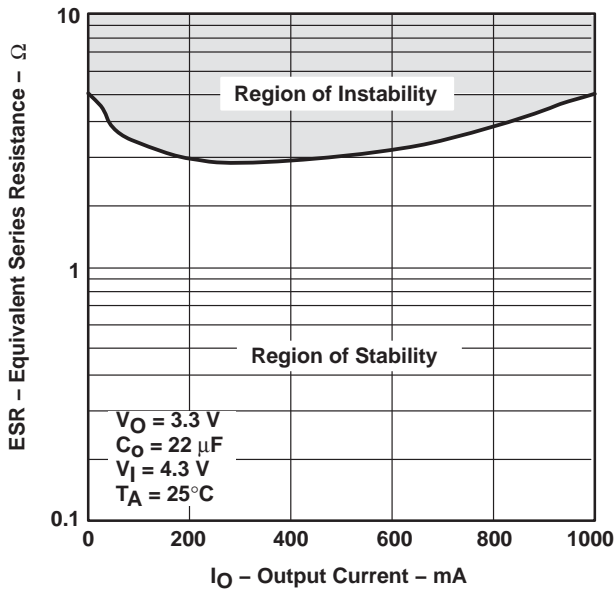


Figure 24

TYPICAL REGION OF STABILITY
 EQUIVALENT SERIES RESISTANCE(1)
 vs
 OUTPUT CURRENT

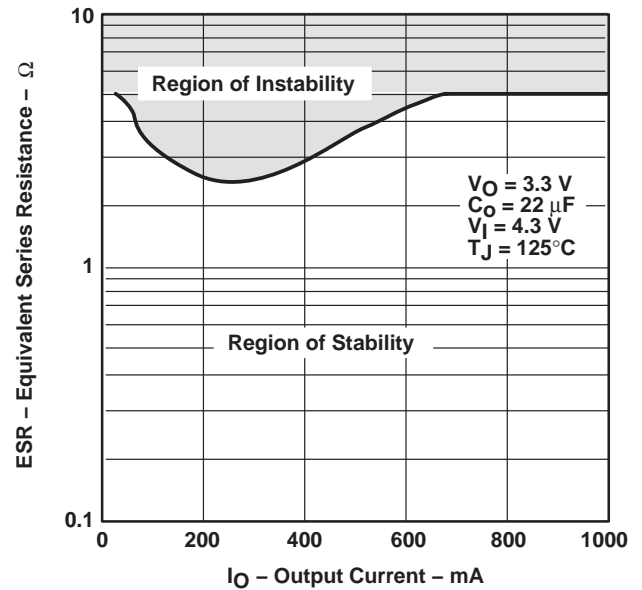


Figure 25

(1) Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

APPLICATION INFORMATION

The TPS767xx family includes eight fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V, 2.7 V, 2.8 V, 3.0 V, 3.3 V, and 5.0 V), and an adjustable regulator, the TPS76701 (adjustable from 1.5 V to 5.5 V).

device operation

The TPS767xx features very low quiescent current, which remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_O/\beta$). The TPS767xx uses a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS767xx quiescent current remains low even when the regulator drops out, eliminating both problems.

The TPS767xx family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to 2 μ A. If the shutdown feature is not used, \overline{EN} should be tied to ground.

minimum load requirements

The TPS767xx family is stable even at zero load; no minimum load is required for operation.

FB—pin connection (adjustable version only)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option. The output voltage is sensed through a resistor divider network to close the loop as shown in Figure 27. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential.

external capacitor requirements

An input capacitor is not usually required; however, a ceramic bypass capacitor (0.047 μ F or larger) improves load transient response and noise rejection if the TPS767xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS767xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 10 μ F and the ESR (equivalent series resistance) must be between 50 m Ω and 1.5 Ω . Capacitor values 10 μ F or larger are acceptable, provided the ESR is less than 1.5 Ω . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 10 μ F surface-mount ceramic capacitors, including devices from Sprague and Kemet, meet the ESR requirements stated above.

APPLICATION INFORMATION

external capacitor requirements (continued)

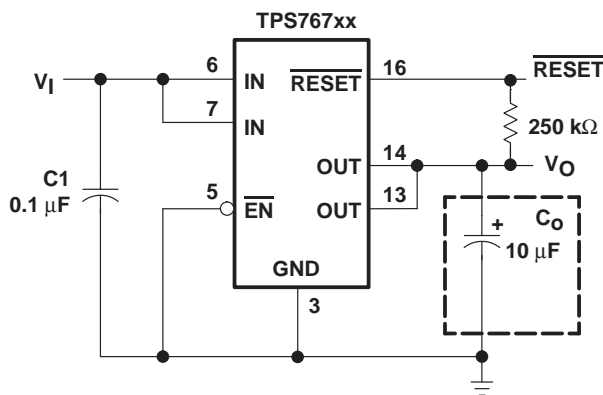


Figure 26. Typical Application Circuit (Fixed Versions)

programming the TPS76701 adjustable LDO regulator

The output voltage of the TPS76701 adjustable regulator is programmed using an external resistor divider as shown in Figure 27. The output voltage is calculated using:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \tag{1}$$

Where:

V_{ref} = 1.1834 V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 50-μA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 50 μA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \tag{2}$$

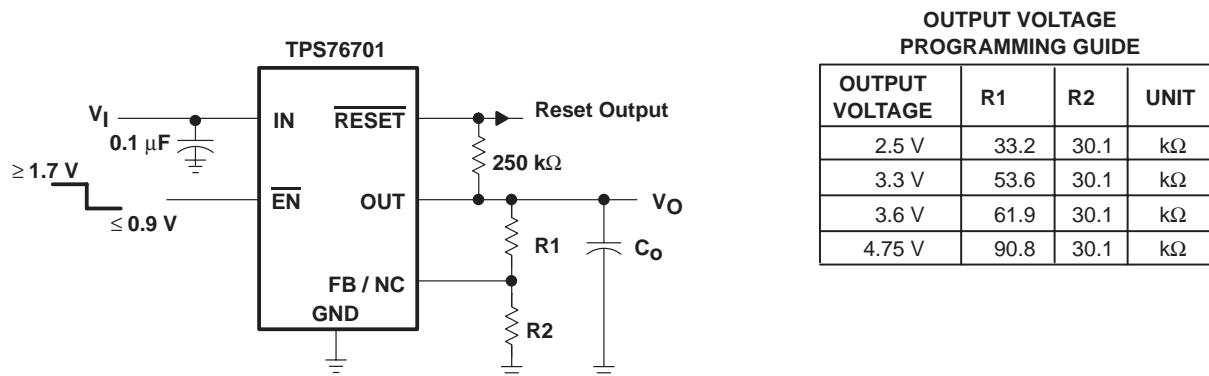


Figure 27. TPS76701 Adjustable LDO Regulator Programming

APPLICATION INFORMATION

reset indicator

The TPS767xx features a $\overline{\text{RESET}}$ output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the $\overline{\text{RESET}}$ output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. $\overline{\text{RESET}}$ can be used to drive power-on reset circuitry or as a low-battery indicator. $\overline{\text{RESET}}$ does not assert itself when the regulated output voltage falls outside the specified 2% tolerance, but instead reports an output voltage low relative to its nominal regulated value (refer to timing diagram for start-up sequence).

regulator protection

The TPS767xx PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS767xx also features internal current limiting and thermal protection. During normal operation, the TPS767xx limits output current to approximately 1.7 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(\text{max})}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(\text{max})}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(\text{max})} = \frac{T_{J\text{max}} - T_A}{R_{\theta\text{JA}}}$$

Where:

$T_{J\text{max}}$ is the maximum allowable junction temperature.

$R_{\theta\text{JA}}$ is the thermal resistance junction-to-ambient for the package, i.e., 172°C/W for the 8-terminal SOIC and 32.6°C/W for the 20-terminal PWP with no airflow.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS76701QD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 76701 | Samples |
| TPS76701QDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 76701 | Samples |
| TPS76701QDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 76701 | Samples |
| TPS76701QDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 76701 | Samples |
| TPS76701QPWP | ACTIVE | HTSSOP | PWP | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT76701 | Samples |
| TPS76701QPWPG4 | ACTIVE | HTSSOP | PWP | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT76701 | Samples |
| TPS76701QPWPR | ACTIVE | HTSSOP | PWP | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT76701 | Samples |
| TPS76701QPWPRG4 | ACTIVE | HTSSOP | PWP | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT76701 | Samples |
| TPS76715QD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 76715 | Samples |
| TPS76715QDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 76715 | Samples |
| TPS76715QPWP | ACTIVE | HTSSOP | PWP | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT76715 | Samples |
| TPS76715QPWPG4 | ACTIVE | HTSSOP | PWP | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT76715 | Samples |
| TPS76718-W | ACTIVE | WAFERSALE | YS | 0 | | TBD | Call TI | Call TI | | | Samples |
| TPS76718QD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 76718 | Samples |
| TPS76718QDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 76718 | Samples |
| TPS76718QDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 76718 X | Samples |
| TPS76718QPWP | ACTIVE | HTSSOP | PWP | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT76718 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS76718QPWPG4 | ACTIVE | HTSSOP | PWP | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT76718 | Samples |
| TPS76718QPWPR | ACTIVE | HTSSOP | PWP | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT76718 | Samples |
| TPS76725QD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 76725 | Samples |
| TPS76725QDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 76725 | Samples |
| TPS76725QDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 76725 | Samples |
| TPS76725QDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 76725 | Samples |
| TPS76725QPWP | ACTIVE | HTSSOP | PWP | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT76725 | Samples |
| TPS76725QPWPG4 | ACTIVE | HTSSOP | PWP | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT76725 | Samples |
| TPS76725QPWPR | ACTIVE | HTSSOP | PWP | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT76725 | Samples |
| TPS76725QPWPRG4 | ACTIVE | HTSSOP | PWP | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT76725 | Samples |
| TPS76727QD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 76727 | Samples |
| TPS76727QPWP | ACTIVE | HTSSOP | PWP | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT76727 | Samples |
| TPS76728QD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 76728 | Samples |
| TPS76728QPWP | ACTIVE | HTSSOP | PWP | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT76728 | Samples |
| TPS76730QD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 76730 | Samples |
| TPS76730QDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 76730 | Samples |
| TPS76730QPWP | ACTIVE | HTSSOP | PWP | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT76730 | Samples |
| TPS76730QPWPG4 | ACTIVE | HTSSOP | PWP | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT76730 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS76730QPWPR | ACTIVE | HTSSOP | PWP | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT76730 | Samples |
| TPS76733QD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 76733 | Samples |
| TPS76733QDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 76733 | Samples |
| TPS76733QDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 76733 | Samples |
| TPS76733QPWP | ACTIVE | HTSSOP | PWP | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT76733 | Samples |
| TPS76733QPWPG4 | ACTIVE | HTSSOP | PWP | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT76733 | Samples |
| TPS76733QPWPR | ACTIVE | HTSSOP | PWP | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT76733 | Samples |
| TPS76733QPWPRG4 | ACTIVE | HTSSOP | PWP | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT76733 | Samples |
| TPS76750QD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 76750 | Samples |
| TPS76750QDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 76750 | Samples |
| TPS76750QDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 76750 | Samples |
| TPS76750QDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 76750 | Samples |
| TPS76750QPWP | ACTIVE | HTSSOP | PWP | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT76750 | Samples |
| TPS76750QPWPG4 | ACTIVE | HTSSOP | PWP | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT76750 | Samples |
| TPS76750QPWPR | ACTIVE | HTSSOP | PWP | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT76750 | Samples |
| TPS76750QPWPRG4 | ACTIVE | HTSSOP | PWP | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PT76750 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS76701, TPS76715, TPS76718, TPS76725, TPS76733, TPS76750 :

- Automotive: [TPS76701-Q1](#), [TPS76715-Q1](#), [TPS76718-Q1](#), [TPS76725-Q1](#), [TPS76733-Q1](#), [TPS76750-Q1](#)
- Enhanced Product: [TPS76701-EP](#), [TPS76715-EP](#), [TPS76718-EP](#), [TPS76725-EP](#), [TPS76733-EP](#), [TPS76750-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|-----------------------------------------------------------|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS76701QDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS76701QPWPR | HTSSOP | PWP | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| TPS76715QDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS76718QDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS76718QPWPR | HTSSOP | PWP | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| TPS76725QDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS76725QPWPR | HTSSOP | PWP | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| TPS76730QPWPR | HTSSOP | PWP | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| TPS76733QDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS76733QPWPR | HTSSOP | PWP | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| TPS76750QDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS76750QPWPR | HTSSOP | PWP | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS76701QDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| TPS76701QPWPR | HTSSOP | PWP | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| TPS76715QDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| TPS76718QDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| TPS76718QPWPR | HTSSOP | PWP | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| TPS76725QDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| TPS76725QPWPR | HTSSOP | PWP | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| TPS76730QPWPR | HTSSOP | PWP | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| TPS76733QDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| TPS76733QPWPR | HTSSOP | PWP | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| TPS76750QDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| TPS76750QPWPR | HTSSOP | PWP | 20 | 2000 | 367.0 | 367.0 | 38.0 |

MECHANICAL DATA

PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE



4073225-4/1 05/11

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

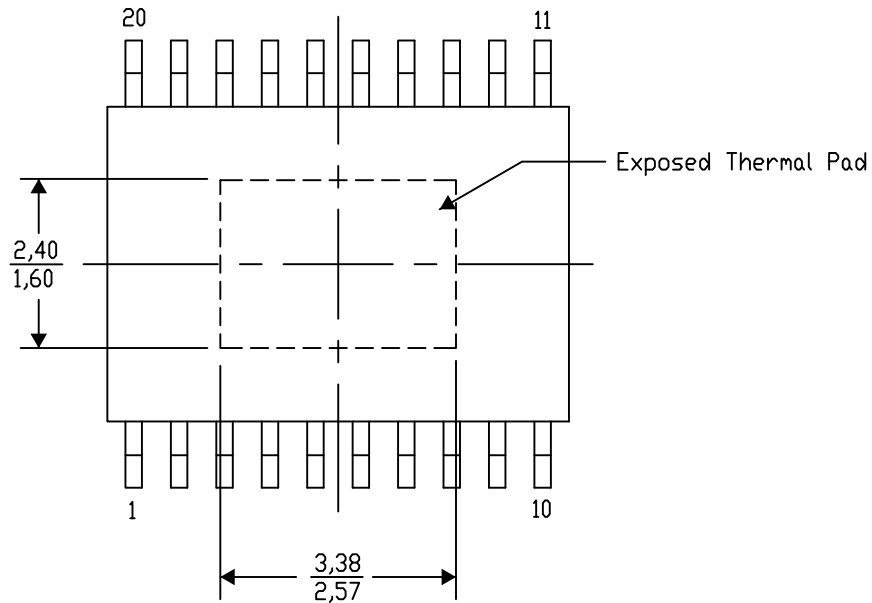
PWP (R-PDSO-G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

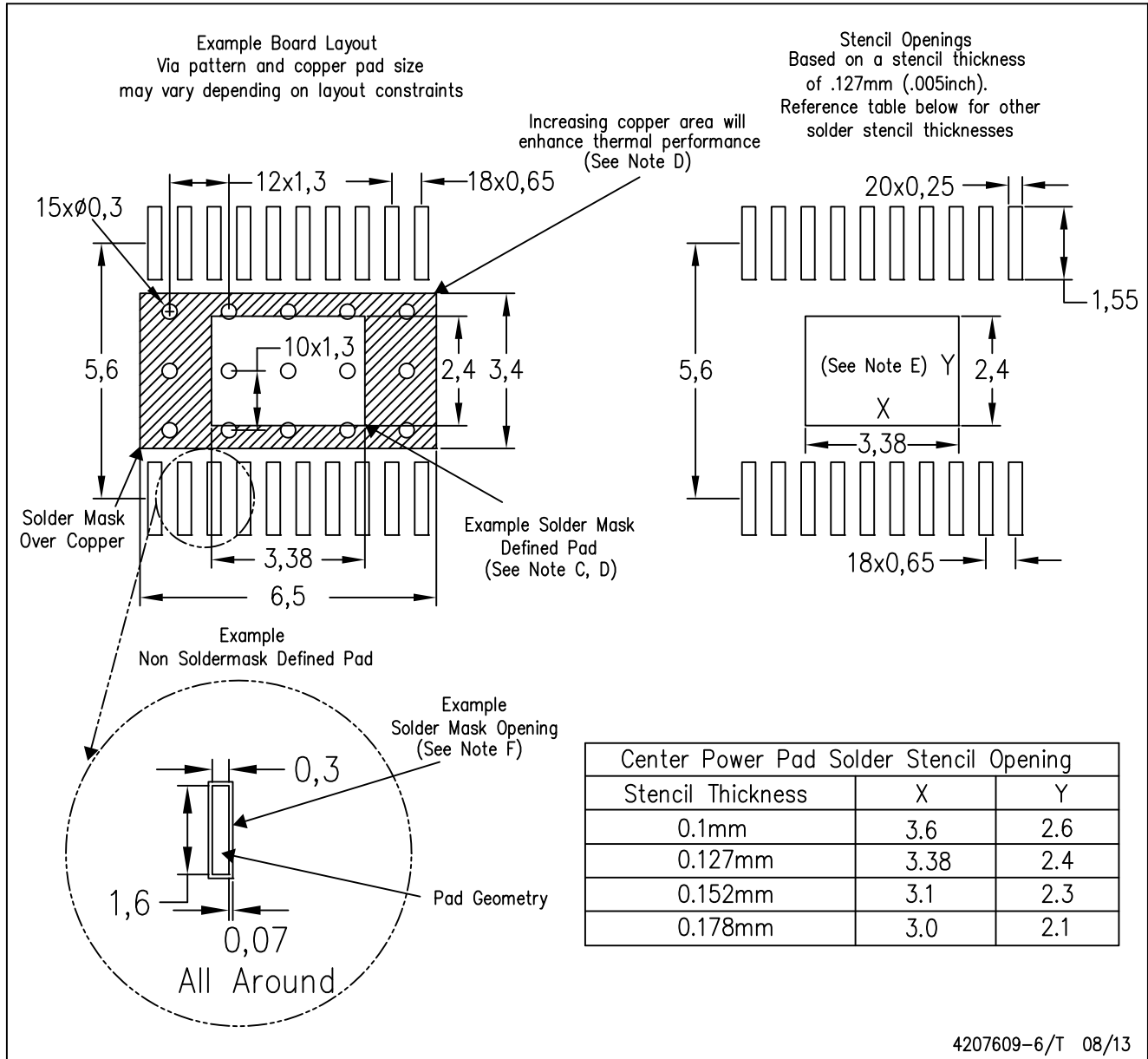
4206332-13/AH 11/13

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

THERMAL PAD MECHANICAL DATA

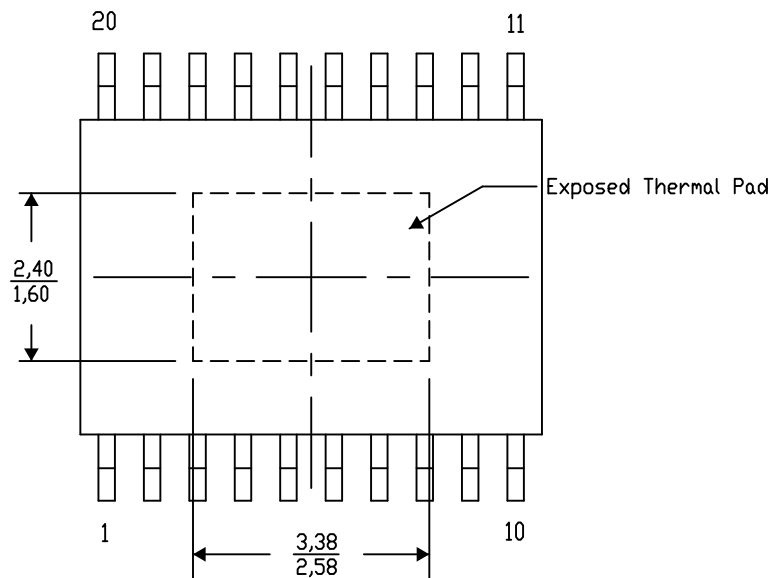
PWP (R-PDSO-G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

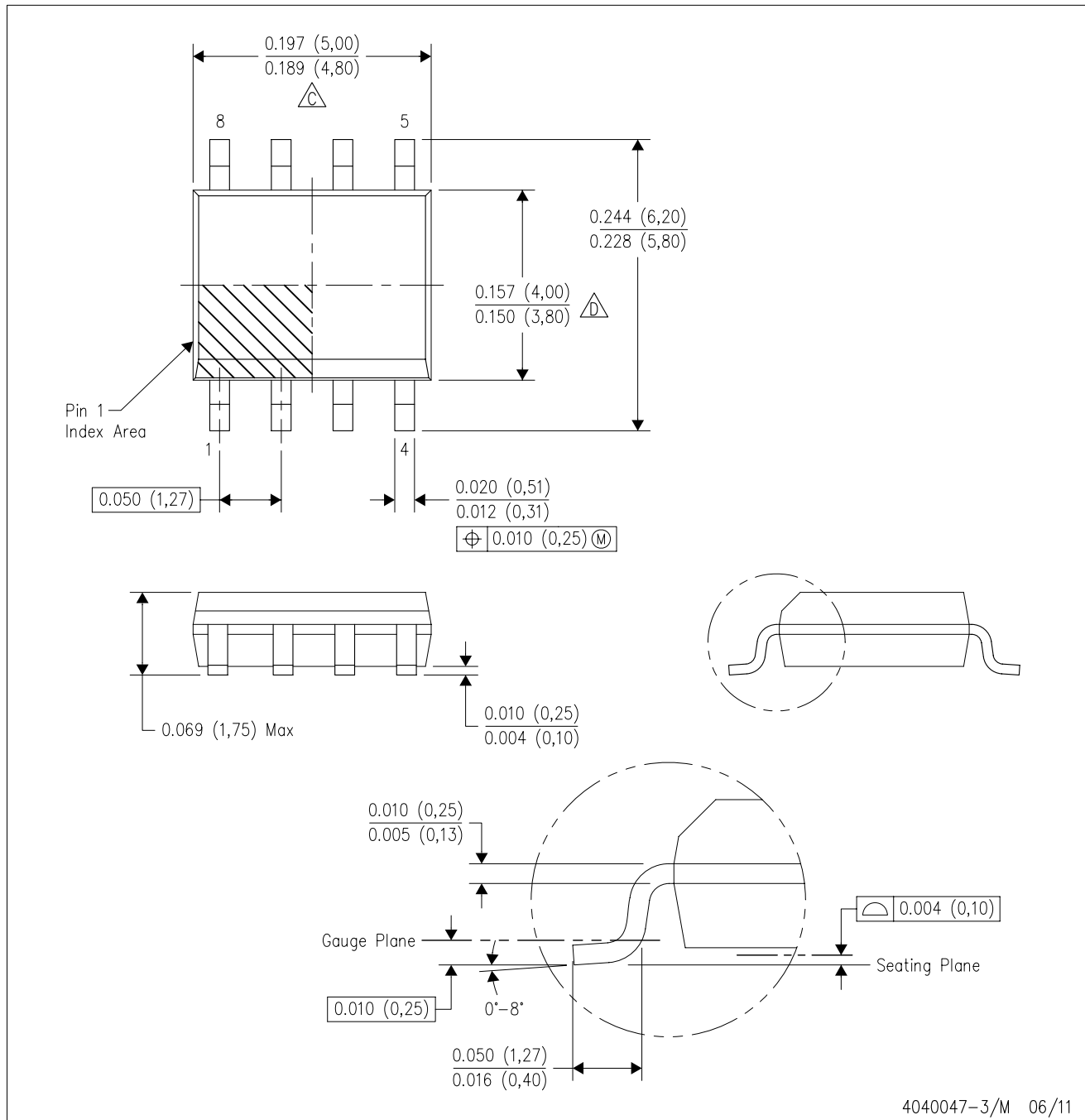
4206332-21/AH 11/13

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

D (R-PDSO-G8)

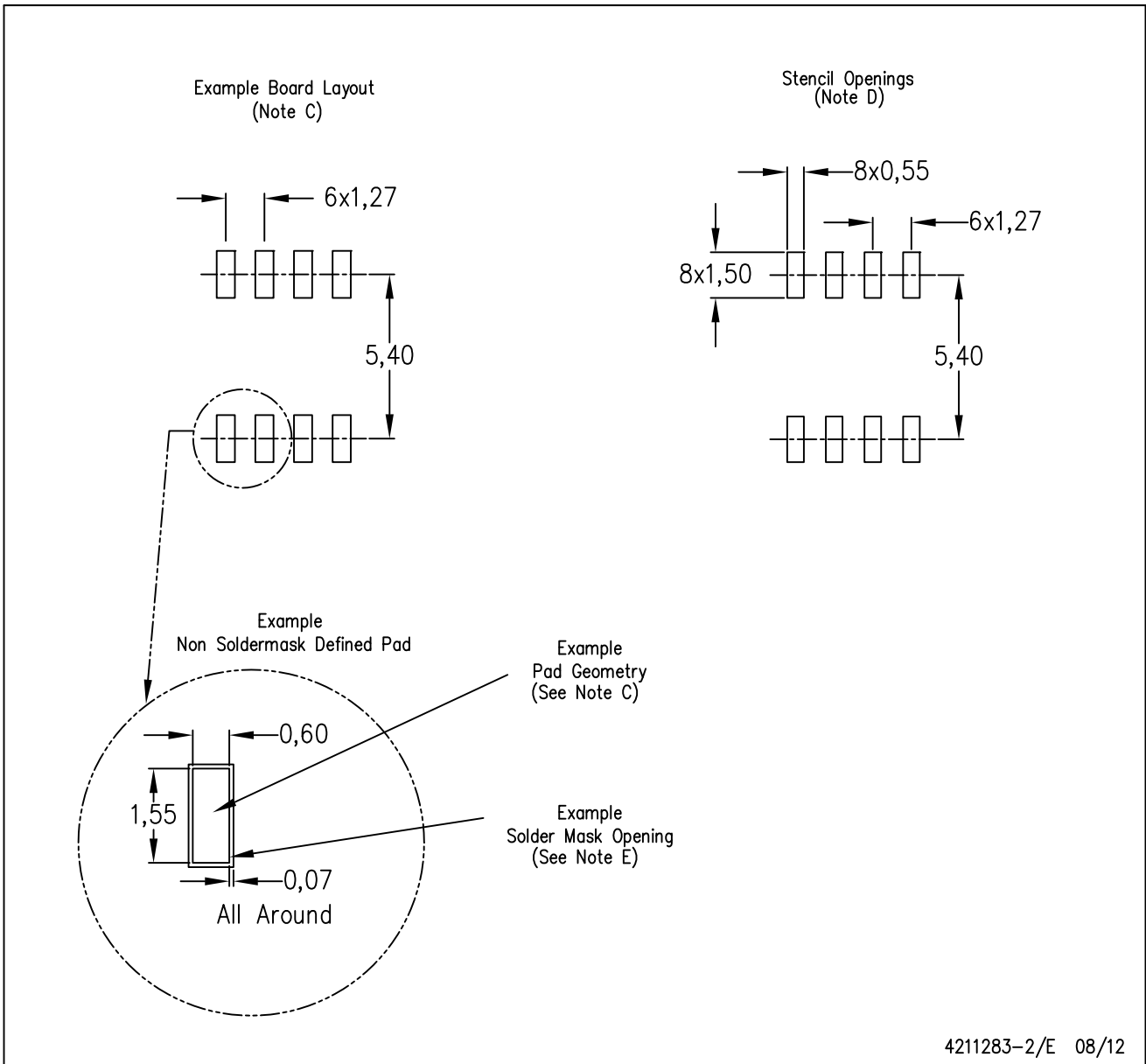
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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